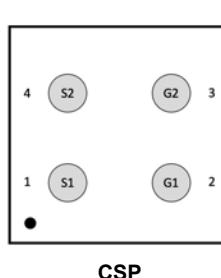
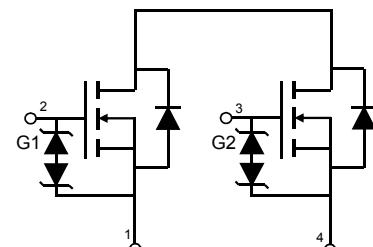


## Main Product Characteristics

$V_{SSS}$	20V
$R_{SS(ON)} \text{ TYP}$	22.6mΩ @4.5V
	22.9mΩ @4.1V
	23.1mΩ @4.0V
	23.3mΩ @3.8V
	23.6mΩ @3.7V
	25.0mΩ @3.1V
	27.7mΩ @2.5V
$I_S$	3.5A



CSP



Schematic Diagram



## Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery

## Description

The GSFCP0204 utilizes the latest techniques to achieve high cell density, low on-resistance and low gate charge. Embedded with ESD diodes, this device is extremely efficient and reliable for use as a load switch and battery protection application.

## Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Max.	Unit
Source-Source Voltage	$V_{SSS}$	20	V
Gate-Source Voltage	$V_{GSS}$	$\pm 12$	V
Source Current (DC) <sup>1</sup>	$I_S$	3.5	A
Source Current (Pulsed) <sup>1,2</sup>	$I_{SP}$	35	A
Total Power Dissipation <sup>1</sup>	$P_T$	2.5	W
Channel Temperature Range	$T_{ch}$	+150	°C
Storage Temperature Range	$T_{STG}$	-55 To +150	°C

**Electrical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>Static Parameters</b>						
Source-Source Breakdown Voltage	$\text{BV}_{\text{SSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=1\text{mA}$	20	-	-	V
Zero Gate Voltage Source Current	$I_{\text{SSS}}$	$V_{\text{SS}}=16\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate-Source Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}=\pm 10\text{V}, V_{\text{SS}}=0\text{V}$	-	-	$\pm 10$	$\mu\text{A}$
Gate to Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{SS}}=V_{\text{GS}}, I_{\text{S}}=250\mu\text{A}$	0.5	0.80	1.3	V
Source to Source On-Resistance	$R_{\text{SS}(\text{ON})}$	$V_{\text{GS}}=4.5\text{V}, I_{\text{S}}=2\text{A}$	15.8	22.6	31	$\text{m}\Omega$
		$V_{\text{GS}}=4.1\text{V}, I_{\text{S}}=2\text{A}$	16.0	22.9	33	
		$V_{\text{GS}}=4.0\text{V}, I_{\text{S}}=2\text{A}$	16.2	23.1	34	
		$V_{\text{GS}}=3.8\text{V}, I_{\text{S}}=2\text{A}$	16.3	23.3	35	
		$V_{\text{GS}}=3.7\text{V}, I_{\text{S}}=2\text{A}$	16.5	23.6	36	
		$V_{\text{GS}}=3.1\text{V}, I_{\text{S}}=2\text{A}$	17.5	25.0	39	
		$V_{\text{GS}}=2.5\text{V}, I_{\text{S}}=2\text{A}$	19.4	27.7	48	
Turn-On Delay Time <sup>3</sup>	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=9\text{V}, R_{\text{L}}=2.8\Omega$ $V_{\text{GS}}=4.5\text{V}$	-	113	-	$\text{nS}$
Turn-On Rise Time <sup>3</sup>	$t_{\text{r}}$		-	246	-	
Turn-Off Delay Time <sup>3</sup>	$t_{\text{d}(\text{off})}$		-	1160	-	
Turn-Off Fall Time <sup>3</sup>	$t_{\text{f}}$		-	516	-	
Input Capacitance	$C_{\text{iss}}$	$V_{\text{SS}}=10\text{V}, V_{\text{GS}}=0\text{V}$ $f=1\text{KHz}$	-	644	-	$\text{pF}$
Output Capacitance	$C_{\text{oss}}$		-	150	-	
Reverse Transfer Capacitance	$C_{\text{rss}}$		-	109	-	
Total Gate Charge <sup>3</sup>	$Q_{\text{g}}$	$V_{\text{SS}}=10\text{V}, V_{\text{GS}}=6\text{V}$ $I_{\text{S}}=3.4\text{A}$	-	8.6	-	$\text{nC}$
Gate 1 - Source 1 Charge <sup>3</sup>	$Q_{\text{g1s1}}$		-	0.9	-	
Gate 1 - Source 2 Charge <sup>3</sup>	$Q_{\text{g1s2}}$		-	2.5	-	
Diode Forward Voltage	$V_{\text{F(S-S)}}$	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=2\text{A}$	-	-	1	V

**Notes:**

1. Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm) using the minimum recommended pad size (36 $\mu\text{m}$  Copper).
2. t=10ms, Duty Cycle  $\leq 1\%$ .
3. When FET1 is measured, G2 and S2 are short-circuited.

## Typical Electrical and Thermal Characteristic Curves

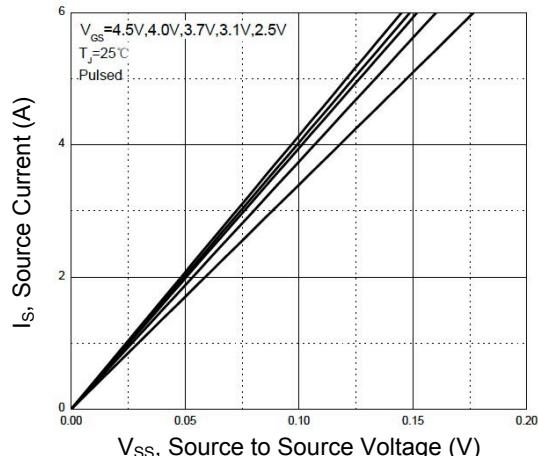


Figure 1. Output Characteristics

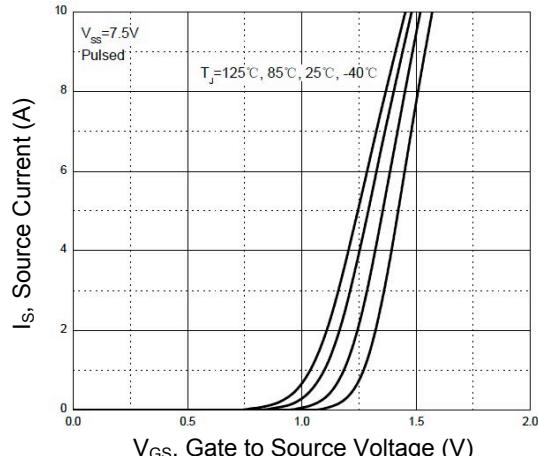


Figure 2. Transfer Characteristics

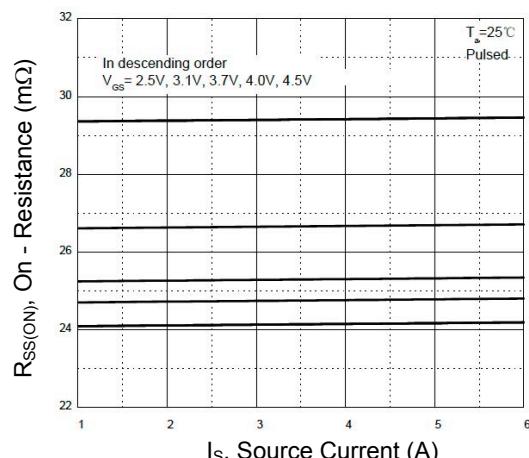


Figure 3.  $R_{SS(ON)}$  vs. Source Current

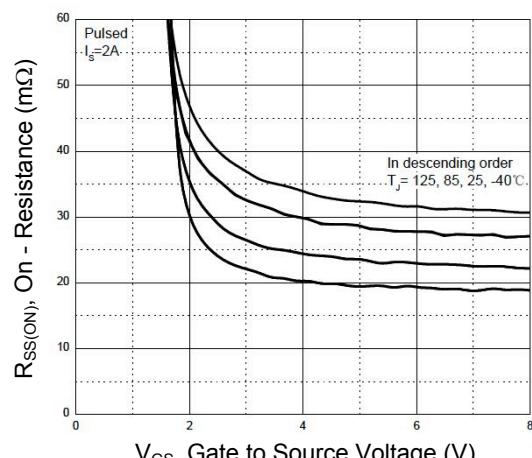


Figure 4.  $R_{SS(ON)}$  vs. Gate to Source Voltage

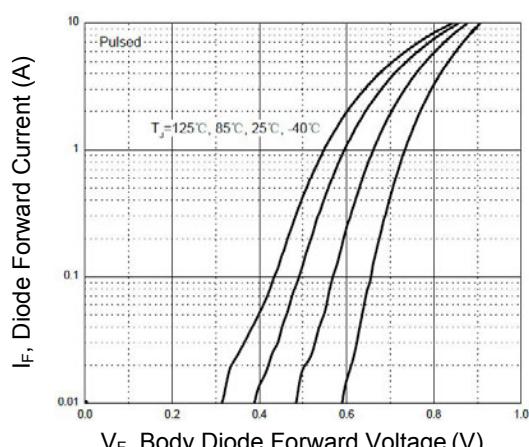


Figure 5. Forward Current vs. Forward Voltage

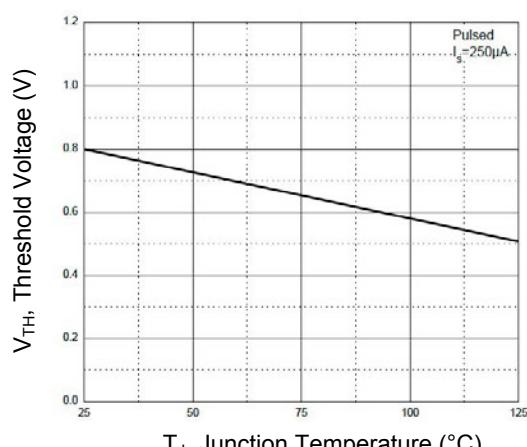


Figure 6. Threshold Voltage vs. Junction Temperature

## Typical Electrical and Thermal Characteristic Curves

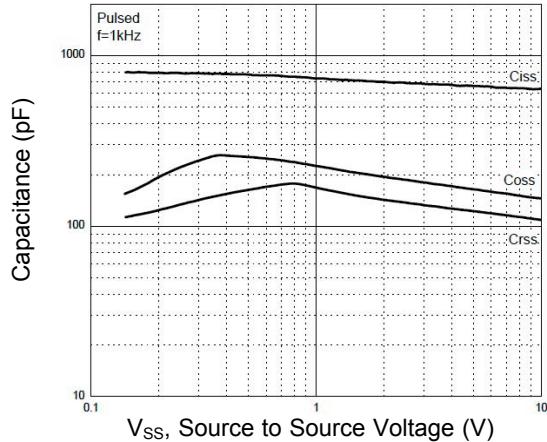


Figure 7. Capacitance Characteristics

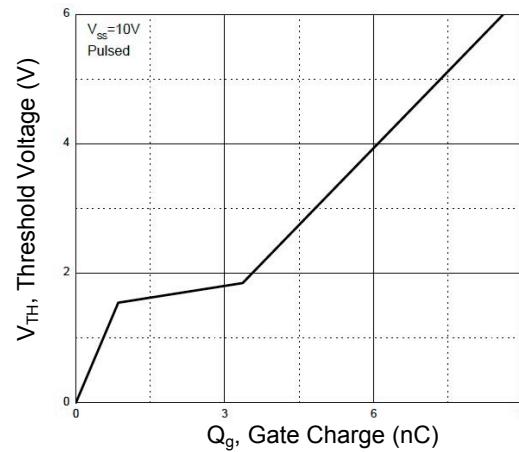


Figure 8. Gate Charge Characteristics

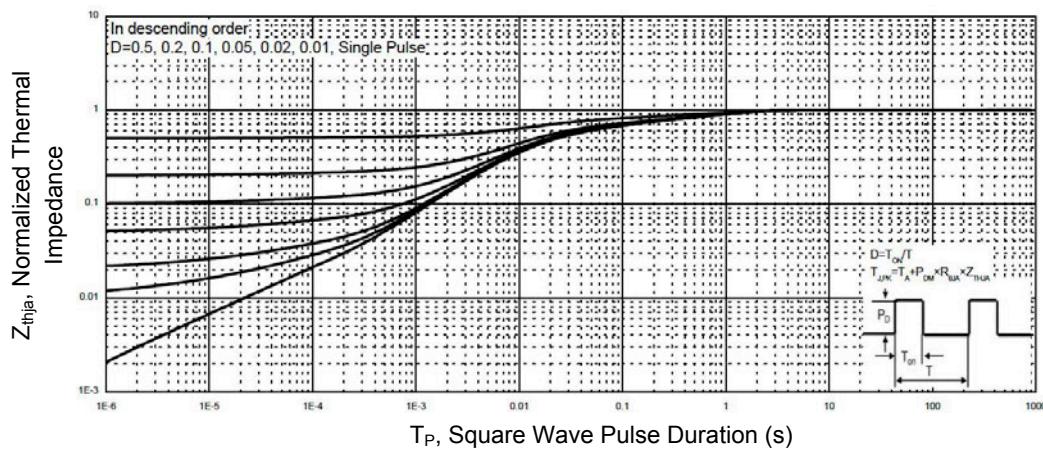


Figure 9. Normalized Maximum Transient Thermal Impedance

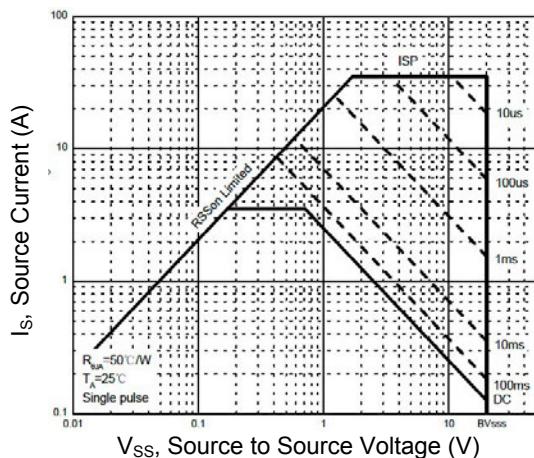
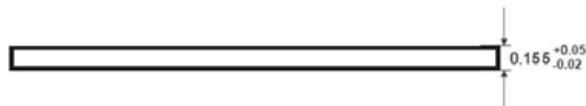
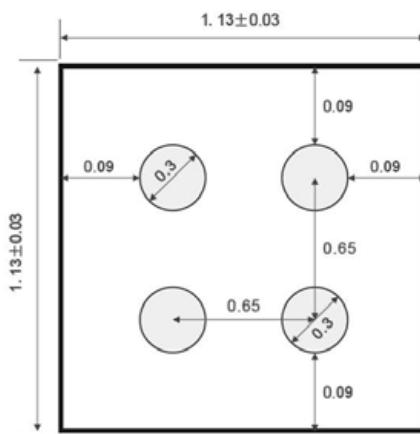
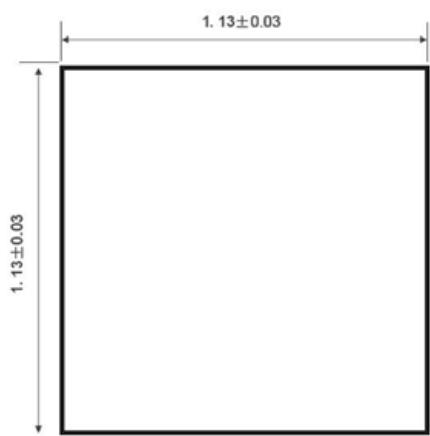


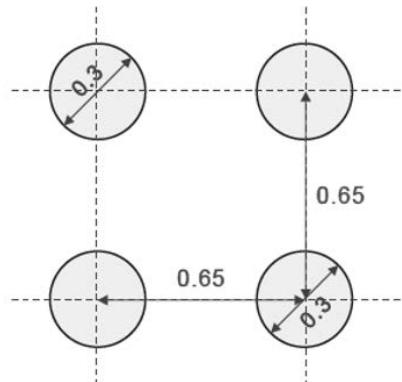
Figure 10. Maximum Forward Biased Safe Operating Area

## Package Outline Dimensions (CSP)

Unit: mm



## Recommended Pad Layout



### Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.050mm.
3. The pad layout is for reference purposes only.